**ECE -1 Lab **

**Experiment - 4**

**Aim:** Implementation of CMOs circuits using DSCH and Microwind

Description: Implement the given circuits at transistor level using 90nm technology.

Section 1:

1. Implement a 2x1 multiplexer using transmission gate approach.
   1. Input sequences for simulation: I0 = 0101010110, I1 = 0001110001 and S = 0011001100. Clock period = 10ns.
2. Implement a 4x1 multiplexer using 2x1 as a user defined symbol.
   1. Input sequences for simulation: I0 = 0101010110, I1 = 0001110001, I2 = 1111100000, I3 = 1100110011, S1 = 0011001100, S0 - 0101010101. Clock period = 10ns.
3. Implement the function F (A, B, C, D) = ∑(1,3,6,8,9,12) using pseudo NMOS logic.
   1. Generate all 16 cases in your test waveform and show the output by taking clock for MSB at 10MHz.

Section 2:

1. For each part in section 1, implement the circuit at transistor level using 90nm technology in DSCH 3.5.
2. Compile the corresponding Verilog file in Microwind and generate the layout file.
3. Simulate the layout file by testbench by considering corresponding cases.
4. Study the delay, power and cell usage for each part.